REMARKS/ARGUMENTS

In view of the foregoing amendments and the following remarks, reconsideration of the above referenced application is respectfully requested.

Claims 55 stands rejected under 35 USC §112, second paragraph. The claim has been amended to provide positive antecedent basis.

Claims 24-47, 50-53, 55-57, and 59 stand rejected under 35 USC §102 (e) as being anticipated by Conway et al, U.S. Patent No. 6,425,033 B1.

Claims 48 and 49 stand rejected under 35 USC §103 (a) as being unpatentable over Conway in view of Hong.

Independent claim 24 has been amended to recite that the circuit is adapted to serially send the bus data "as a data transaction" .... without requiring or waiting for an incoming acknowledgement over the link before inaugurating a transfer of "the bus data as another data transaction" over the link. In contrast, Conway provides for Success Acknowledgements and Failure Acknowledgements after a data transaction, such as after a Posted Write Transaction described in column 10 lines 8 - column 12 line 8. As previously discussed in Applicant's previous Response, the Conway serial data transmission scheme creates significant latency due to these Success Acknowledgements and Failure Acknowledgments. Conway even acknowledges that his scheme does not operate at the full performance required by the PCI bus, stating "although this serial link increases the latency of the first piece of information transferred, the aggregate bit rate is fast enough to maintain sustained performance close to that achieved by

the PCI bus". (see specification column 9, lines 4-7). During a burst transaction, which notably is not described by Conway, this latency could cause the bridge exchanging PCI transactions to fail. With a burst data read or write cycle, the latency of Conway creates a bottleneck making the bridge prone to failure.

Advantageously, Applicant claimed invention achieves technical advantages in that the claimed circuit and bridge maintains sustained performance to that achieved by the PCI bus, even during burst transactions, which solves the latency problems that designers have been troubled with when trying to design serial bridges for use in PCI systems. Applicant's claimed solution is the first circuit and serial PCI bridge that meets the full performance required by the PCI bus. This is a tremendous technological feet. Support for this feature is found in Applicant's specification on page 19, lines 20-25.

Independent Claim 31 has been amended consistent with independent Claim 24, and thus is believe to define over the prior art as well. A notice to this effect is respectfully requested.

ALLOWABLE SUBJECT MATTER

Claims 54 and 58 are indicated as allowable over the prior art if rewritten in independent form including all the limitations of the base claim and any intervening claims. Accordingly, the limitations of Claim 53 have been amended into dependent Claims 54 and 58, and thus these claims are now in condition of allowance. An additional fee is included for the additional independent claim. Original Claim 53 has been deleted, and the dependency of the remaining

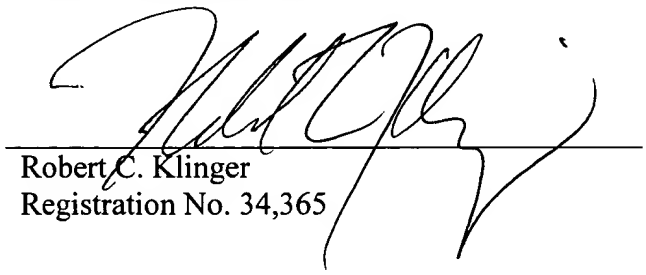
dependent Claims 55 – 57 and 59 now properly depend from allowable independent Claim 54. A notice to this effect is respectfully requested.

A Three Month Extension of Time is included herewith along with the requisite fee.

No additional fees are believed to be due, however, the Examiner is authorized to debit Applicant's Deposit Account #50-1752 if any additional fees are required.

If the Examiner has any further issues, the Examiner is encouraged to contact the undersigned to resolve these matters by phone where possible.

Respectfully Submitted,



Robert C. Klinger
Registration No. 34,365

Jackson Walker L.L.P.
901 Main Street, Suite 6000
Dallas, TX 75202
(214) 953-5978 - Direct Dial
(214) 661-6873 - Direct Fax